WHAT IS CLAIMED IS:

1. A method for producing data from an information signal comprising:

receiving a test signal;

delaying said test signal by increasing amounts of delay times to produce a plurality of delayed test signals, each delayed test signal having an associated delay number corresponding to its delay time, said delay number arranged in increasing order of delay time;

evaluating each delayed test signal for an error condition;

reading one or more adjustment values from a first memory store, said adjustment values being received into said first memory store from an external source and so are variable;

producing a first delay value by combining one or more of said delay times with said one or more adjustment values, including selecting one or more of said delay times based on those of said delayed test signals for which error conditions occur;

receiving a transmission of said information signal; and

delaying said information signal by an amount of time depending on said first delay value, wherein said information signal becomes synchronized with a clock signal used to produce data from said information signal.

2. The method of claim 1 wherein said producing a first delay value includes:

detecting a delay time P0 associated with the smallest delay number for which its corresponding delayed test signal has an error condition;

detecting a delay time P1 associated with the smallest delay number for which its corresponding delayed test signal has an error condition and for which the next larger delay number has a corresponding delayed test signal that does not have an error condition;

detecting a delay time P2 associated with the largest delay number for which its corresponding delayed test signal has an error condition and for which the previous smaller delay number has a corresponding delayed test signal that does not have an error condition;

combining said delay time P0 with one or more of said adjustment values to produce said first delay value if said combining results in a value greater than zero;

if said combining results in a value less than or equal to zero and said delay time P2 exists, then producing said first delay value as a function of said delay times P1 and P2 with one or more of said adjustment values; and

if said combining results in a value less than or equal to zero and said delay time P2 does not exist, then combining said delay time P1 with one or more of said adjustment values to produce said first delay value.

3. The method of claim 1 wherein said evaluating includes performing a parity check.

4. The method of claim 1 wherein said adjustment values include one or more of: one or more factors based on power-supply noise; one or more factors based on device temperature; and one or more factors based on process variations.

5. The method of claim 1 further including:

reading at least one additional adjustment value from a second memory store to produce a second delay value based on said first delay value and on said at least one additional adjustment value, said second memory store either being the same as or different from said first memory store;

receiving a control signal that is associated with said information signal; and

delaying said control signal by an amount of time depending on said second delay value, wherein said information signal and said control signal may be delayed by different amounts of time.

6. The method of claim 1 further including:

producing a transmission delay value including reading one or more delay-time values contained in a second memory store; and

transmitting said information signal as said transmission of said information signal, including delaying said information signal by an amount of time depending on said transmission delay value.

7. The method of claim 1 as embodied in a device comprising a plurality of substantially identical data circuits, each data circuit operating in accordance with said method.

8. The method of claim 1 as embodied in a device comprising a plurality of chips, each chip comprising one or more identical data circuits, each data circuit operating in accordance with said method.

9. A data circuit system comprising:

a plurality of input data lines for receiving data signals, including test signals;

a first plurality of delay circuits having inputs and outputs, said input data lines coupled to said inputs thereof, said delay circuits configured to produce a delayed data signal, said delay circuits further configured, in response to receiving said test signals, to produce a plurality of delayed test signals each having a different delay time, each delayed test signal having an associated delay number corresponding to its delay time, said delay number arranged in increasing order of delay time;

a data error checking unit coupled to receive said outputs of said first plurality of delay circuits and to produce data error indication signals;

a first rewrite-able memory to store adjustment values, said memory having an input for receiving externally-provided values, said adjustment values thereby being updatable depending on said externally-provided values; and

delay-time generation logic configured to produce a first data delay signal indicative of a first data delay time by combining one or more of said delay times with said one or more adjustment values, including selecting one or more of said delay times based on those of said delayed test signals for which error conditions occur, and having an output to output said first data delay signal,

said first plurality of delay circuits having delay control inputs coupled to receive said first data delay signal so as to delay said data signals by an amount of time substantially equal to said first data delay time.

10. The data circuit system of claim 9 wherein said delay-time generation logic comprises:

first logic circuits configured to receive a delay time P0 associated with the smallest delay number for which its corresponding delayed test signal has an error condition, a delay time P1 associated with the smallest delay number for which its corresponding delayed test signal has an error condition and for which the next larger delay number has a corresponding delayed test signal that does not have an error condition, and a delay time P2 associated with the largest delay number for which its corresponding delayed test signal has an error condition and for which the previous smaller delay number has a corresponding delayed test signal that does not have an error condition;

second logic circuits configured to combine said delay time P0 with one or more of said adjustment values to produce a first candidate value;

third logic circuits configured to combine said delay time P1 with one or more of said adjustment values to produce a second candidate value;

fourth logic circuits configured to produce an alternate second candidate value as a function of said delay times P1 and P2 with one or more of said adjustment values;

fifth selection logic configured to select said first candidate value as said first data delay time if said first candidate value is greater than zero;

sixth selection logic configured to select said second candidate value as said first data delay time if said first candidate value is less than or equal to zero and if said delay time P2 is determined to be non-existent; and

seventh selection logic configured to select said alternate second candidate value as said first data delay time if said first candidate value is less than or equal to zero and if said delay time P2 is determined to exist.

11. The data circuit system of claim 9 wherein said data error checking unit comprises parity checking logic.

12. The data circuit system of claim 9 wherein said adjustment values include one or more of: one or more factors based on power-supply noise; one or more factors based on device temperature; and one or more factors based on process variations.

13. The data circuit system of claim 9 further including:

one or more control lines;

a second plurality of delay circuits having inputs and outputs, said control lines coupled to said inputs thereof, said outputs thereof producing delayed control signals; and

a second rewrite-able memory for storing at least one additional adjustment value,

said delay-time generation logic further having a second output to produce a second data delay signal indicative of a second data delay time, said second data delay time being a function of said first data delay time and said at least one additional adjustment value,

said second plurality of delay circuits having delay control inputs coupled to receive said second data delay signal output, thereby producing said delayed control signals.

14. The data circuit system of claim 9 further including an information transmitting circuit comprising:

a second plurality of delay circuits;

a second rewrite-able memory to store a transmission delay value, said memory having an input for receiving externally-provided values, said transmission delay value thereby being updateable depending on said externally-provided values; and

logic operatively coupled to said second rewrite-able memory and configured to produce a transmission delay signal based on said transmission delay value,

said second plurality of delay circuits configured to receive said transmission delay signal,

said second plurality of delay circuits configured to receive information for transmission,

said information for transmission being delayed by an amount corresponding to said transmission delay signal.

15. The data circuit system of claim 9 as incorporated in a device comprising a plurality of said data circuit systems.

16. The data circuit system of claim 9 as incorporated in a device comprising a plurality of chips, each chip having one or more of said data circuit systems.

17. A data circuit system comprising:

means for receiving data signals, said data signals including test signals;

means for delaying said data signals by a variable delay amount;

means for detecting errors in received data signals;

first means for receiving externally provided values and storing them as first adjustment values; and

means for producing one or more first delay control signals representative of a first delay value, including first means for producing one or more candidate delay values based on errors detected by said means for detecting and on said first adjustment values, said first delay value being one of said one or more candidate delay values,

said one or more first delay control signals coupled to said means for delaying said data signals to delay said data signals by an amount of time substantially equal to said first delay value.

18. The data circuit system of claim 17 further including:

means for receiving a control signal associated with said data signals;

means for delaying said control signal by a variable delay amount; and

second means for receiving externally provided values and storing them as one or more second adjustment values; and

means for combining said first delay value and said one or more second adjustment values to produce a second delay control signal representative of a second delay value,

said delay control signal coupled to said means for delaying said control signal to delay said control signal by an amount to time substantially equal to said second delay value.

19. The data circuit system of claim 17 further including:

second means for receiving externally provided values and storing them as second adjustment values;

second means for determining a delay value to produce a transmission delay value based on said second adjustment values;

second means for producing one or more second delay control signals from said transmission delay value; and

means for transmitting information signals, including means for delaying transmission of said information signals by an amount of time substantially equal to said transmission delay value,

said information signals including said data signals.

20. The data circuit system of claim 17 as incorporated in a device comprising a plurality of said data circuit systems.